Tab 2

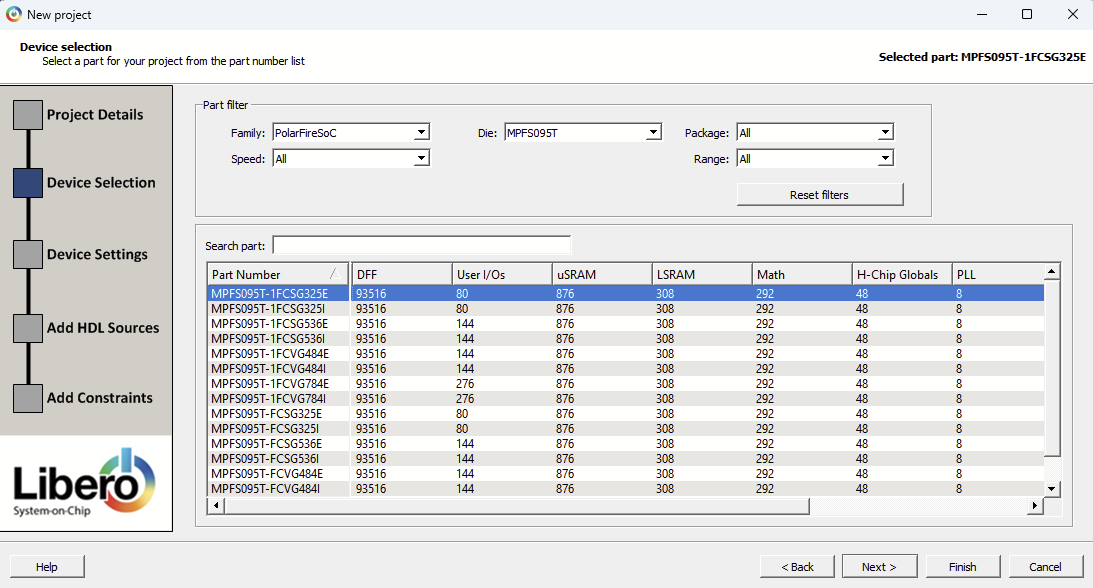
**Creating a project**

1. Go to “Project > New Project” and choose a name and file location

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1. Select the device as shown below



1. At “Device Settings” page, use the defaults and click “Next”
2. “Add HDL Sources” will allow you to start the project with existing HDL source files, but HDL source files can also be added later.
3. We will not use “Add Constraints” during project creation.

**Making a SmartDesign**

1. Select “File > New > SmartDesign”

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1. Name your SmartDesign.
2. Right-click your SmartDesign and click “Set as Root”

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**Adding source files to the SmartDesign**

1. Open the folder “project\_name > hdl” in Visual Studio Code (Lookup how to install VSCode if not already installed)

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1. In Visual Studio Code, make a .sv file in the “hdl” folder by right clicking

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Here is a sample SV file to test:

module blinky( //a module is kind of like a function in other coding languages. This module's name is "blinky"

input logic pushButton, //input logic for input signals (pushButton is the variable (wire) name)

output logic light //output logic for input signals (light is the variable (wire) name)

); //End of port definitions (inputs/outputs)

assign light = pushButton; //this connects the input variable to the output variable

                           //with a physical wire, hence the term "Hardware Description Language"

endmodule //End of the blinky module

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1. In Libero, click “Build Hierarchy” for Libero to recognize the new source file.

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* 1. Libero will only recognize source files that have modules, meaning that the .sv file must have “module…endmodule”

1. Access the SmartDesign by double clicking it in the “Design Hierarchy” tab

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1. In the SmartDesign, drag the module “blinky” onto the workspace to see its ports.

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1. Additional source files can be added to the folder and dragged onto the workspace.

**Adding top-level input/output ports in the SmartDesign**

1. Right-click the workspace and select “Add Port”

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1. Specify input/output and the bit depth ([N-1:0] for N bits)

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1. You can drag to connect a port.

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**Synthesis**

1. In your SmartDesign, click the “Generate Component” icon (looks like a yellow barrel)

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1. Under the “Design Flow” tab, double-click “Synthesize” (under “Implement Design”)

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**Pin Assignment**

1. Under the “Design Flow” tab, double-click “Manage Constraints” (under “Constraints”)

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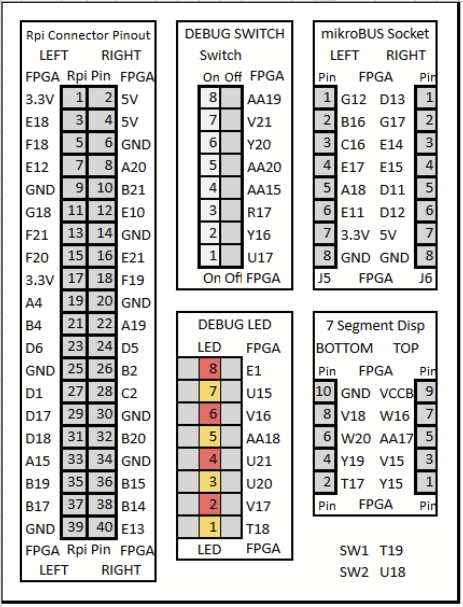
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1. Under “I/O Attributes” click “Edit > Edit with I/O Editor”

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1. Assign each “Pin Number” as shown below (also available in the excel sheet)



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1. In the top left, click the blue commit icon.

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1. Close the I/O editor

**Place and Route**

1. Under the “Design Flow” tab, double-click “Place and Route” (under “Implement Design”)

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**Flash to the FPGA**

1. Connect your PC to the FPGA using a USB-C cable
2. Under the “Design Flow” tab, scroll down and double-click “Run PROGRAM Action” (under “Program Design”)

A screenshot of a computer program

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1. Wait for the FPGA to flash. Once it is done, the left-most LED should turn off when you press push button 1! It is on by default because the buttons are active-low, meaning a logical 0 is represented by a button press and logical 1 by default. Now you are ready to implement more complicated designs!